CLAIMS

What is claimed is:

1. A delay circuit, comprising:

a first circuit having a circuit input to receive a reference signal and a circuit output to output a delayed signal;

a falling edge delay circuit coupled to the first circuit to control delay of a falling edge of the reference signal; and

a rising edge delay circuit coupled to the first circuit to control delay of a rising edge of the reference signal.

2. The delay circuit of claim 1, wherein the first circuit comprises an enable circuit further including an enable input to enable the delay circuit.

3. The delay circuit of claim 2, wherein the circuit input comprises a clock input to receive a reference clock signal and the reference signal comprises the reference clock signal.

4. The delay circuit of claim 3, wherein the falling edge delay circuit and the rising edge delay circuit are coupled to delay the falling edge and the rising edge independently of each other.

5. The delay circuit of claim 4, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal by variable falling delays and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by variable rising delays.

6. The delay circuit of claim 5, wherein the falling edge delay circuit further comprises falling delay inputs to receive falling delay signals, the falling edge delay circuit to select one of the variable falling delays based on the falling delay signals and wherein the rising edge delay circuit further comprises rising delay inputs to receive rising delay signals, the rising edge delay circuit to select one of the variable rising delays based on the rising delay signals.

7. The delay circuit of claim 5, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal by one of four falling delays in linear increments, and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by one of four rising delays in linear increments.

8. The delay circuit of claim 6, wherein the enable circuit comprises:

a NAND logic gate having first and second NAND inputs and a NAND output, the first NAND input coupled to the clock input and the second NAND input coupled to the enable input;

a first pull up path including a first transistor to selectively couple the NAND output to the falling edge delay circuit;

a pull down path including second and third transistors coupled in series to selectively couple the NAND output to the rising edge delay circuit; and

an inverter coupling the NAND output to the circuit output.

9. The delay circuit of claim 8, wherein the falling edge delay circuit comprises three parallel pull up paths each including at least one transistor to be coupled between a supply voltage and the first pull up path of the enable circuit, each one of the three parallel pull up paths responsive to the falling delay signals to select one of the variable falling delays.

10. The delay circuit of claim 8, wherein the rising edge delay circuit comprises three parallel pull down paths each including at least one transistor to be coupled between a ground voltage and the first pull down path of the enable circuit, each one of the three parallel pull down paths responsive to the rising delay signals to select one of the variable rising delays.

11. The delay circuit of claim 4, wherein the enable circuit is an inverting enable circuit to invert the reference clock signal, the inverting enable circuit comprising:

a NAND logic gate having first and second NAND inputs and a NAND output, the second NAND input coupled to the enable input;

a first inverter coupling the clock input to the first NAND input;

a pull up path including a first transistor to selectively couple the NAND output to the rising edge delay circuit;

a pull down path including second and third transistors coupled in series to selectively couple the NAND output to the falling edge delay circuit; and

an second inverter coupling the NAND output to the circuit output.

12. The delay circuit of claim 11, wherein the rising edge delay circuit comprises three parallel pull up paths each including at least one transistor to be coupled between a supply voltage and the first pull up path of the enable circuit, each one of the three parallel pull up paths responsive to rising delay inputs of the rising edge delay circuit to select one of variable falling delays of the output delayed signal.

13. The delay circuit of claim 11, wherein the falling edge delay circuit comprises three parallel pull down paths each including at least one transistor to be coupled between a ground voltage and the first pull down path of the enable circuit, each one of the three parallel pull down paths responsive to falling delay inputs of the falling edge delay circuit to select one of variable rising delays of the output delayed signal.

14. A machine-accessible medium having contained thereon a description of an integrated circuit, the integrated circuit comprising:

a clock enable circuit having a clock input to receive a reference clock signal, an enable input, and a circuit output to output a delayed clock signal;

a falling edge delay circuit coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and

a rising edge delay circuit coupled to the enable circuit to control delay of a rising edge of the reference clock signal.

15. The machine-accessible medium of claim 14, wherein the falling edge delay circuit and the rising edge delay circuit are coupled to delay the falling edge and the rising edge independently of each other.

16. The machine-accessible medium of claim 15, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal by variable falling delays and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by variable rising delays.

17. The machine-accessible medium of claim 16, wherein the falling edge delay circuit further comprises falling delay inputs to receive falling delay signals, the falling edge delay circuit to select one of the variable falling delays based on the falling delay signals and wherein the rising edge delay circuit further comprises rising delay inputs to receive rising delay signals, the rising edge delay circuit to select one of the variable rising delays based on the rising delay signals.

18. The machine-accessible medium of claim 16, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal

by one of four falling delays in linear increments, and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by one of four rising delays in linear increments.

19. The machine-accessible medium of claim 17, wherein the clock enable circuit comprises:

a NAND logic gate having first and second NAND inputs and a NAND output, the first NAND input coupled to the clock input and the second NAND input coupled to the enable input;

a first pull up path including a first transistor to selectively couple the NAND output to the falling edge delay circuit;

a pull down path including second and third transistors coupled in series to selectively couple the NAND output to the rising edge delay circuit; and

an inverter coupling the NAND output to the circuit output.

20. The machine-accessible medium of claim 19, wherein the falling edge delay circuit comprises three parallel pull up paths each responsive to the falling delay signals to select one of the variable falling delays, and wherein the rising edge delay circuit comprises three parallel pull down paths each responsive to the rising delay signals to select one of the variable rising delays.

21. The machine-accessible medium of claim 14, wherein the description comprises one of hardware behavioral code, register transfer level code, a netlist, and a circuit layout.

22. An integrated circuit, comprising:

a clock distribution network to distribute a reference clock signal throughout the integrated circuit;

clock delay circuits each comprising:

a clock enable circuit having a clock input to receive the reference clock signal and a circuit output to output a delayed clock signal;

a falling edge delay circuit coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and

a rising edge delay circuit coupled to the enable circuit to control delay of a rising edge of the reference clock signal;

latches each clocked according to the delayed clock signal output from each of the clock delay circuits; and

logic clusters to compute logic values, the latches coupled to buffer the logic values between clock edges of the delayed clock signals.

23. The integrated circuit of claim 22, wherein the falling edge delay circuit and the rising edge delay circuit are coupled to delay the falling edge and the rising edge independently of each other.

24. The integrated circuit of claim 22, wherein the falling edge delay circuit further comprises falling delay inputs to receive falling delay signals, the falling edge delay circuit to selectively delay the falling edge of the reference clock signal by one of variable falling delays based on the falling delay signals, and wherein the rising edge delay circuit further comprises rising delay inputs to receive rising delay signals, the rising edge delay circuit to selectively delay the rising edge of the reference clock signal by one of the variable rising delays based on the rising delay signals.

25. The integrated circuit of claim 24, wherein the clock delay circuits are grouped into domains of the integrated circuit, the falling delay inputs and the rising delay inputs of the clock delay circuits coupled to receive the same falling delay signals and the same rising delay signals within each of the domains.

26. The integrated circuit of claim 24, wherein the falling edge delay circuit is further coupled to selectively delay the falling edge of the reference clock signal by one of four falling delays in first increments, and wherein the rising edge delay circuit is further coupled to selectively delay the rising edge of the reference clock signal by one of four rising delays in second increments.

27. The integrated circuit of claim 26, wherein the first and second increments comprise substantially linear increments.

28. The integrated circuit of claim 22, wherein the integrated circuit comprises a microprocessor.

29. The integrated circuit of claim 22, wherein the logic clusters comprise at least one of combinational logic and sequential logic.

30. The integrated circuit of claim 23, wherein the clock enable circuit comprises:

a NAND logic gate having first and second NAND inputs and a NAND output, the first NAND input coupled to the clock input and the second NAND input coupled to the enable input;

a first pull up path including a first transistor to selectively couple the NAND output to the falling edge delay circuit;

a pull down path including second and third transistors coupled in series to selectively couple the NAND output to the rising edge delay circuit; and

an inverter coupling the NAND output to the circuit output.

31. The integrated circuit of claim 30, wherein the falling edge delay circuit comprises three parallel pull up paths each responsive to the falling delay signals to select one of the variable falling delays, and wherein the rising edge delay circuit comprises three parallel pull down paths each responsive to the rising delay signals to select one of the variable rising delays.

32. The integrated circuit of claim 22, wherein the latches comprise flip-flops.